IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended): A liquid crystal display device having an array substrate, comprising:

a substrate;

a gate line and a data line on the substrate, the gate line and the data line crossing each other and defining a pixel area;

a thin film transistor electrically connected to the gate line and the data line, and including:

a gate electrode connected to the gate line;

a source electrode over the gate electrode and connected to the data line;

a drain electrode spaced apart from the source electrode; and

a semiconductor layer having an active layer over the gate electrode, [[and]] a first extended portion, and a neck region connecting the active layer and the first extended portion, wherein the neck region is completely covered with the drain electrode ~~at a boundary between the active electrode and the first extended portion, wherein the first extended portion is disposed over the gate electrode~~; and

a pixel electrode in the pixel region and connected to the drain electrode.

2. (Original): The liquid crystal display device according to claim 1, wherein the source electrode has a U-shape and surrounds a part of the drain electrode.

3. (Original): The liquid crystal display device according to claim 2, wherein the part of the drain electrode has a rod shape.

4. (Original): The liquid crystal display device according to claim 1, further comprising a second extended portion corresponding to the data line in the semiconductor layer.

5. (Original): The liquid crystal display device according to claim 1, wherein the semiconductor layer is formed of amorphous silicon.

6. (Currently Amended): The liquid crystal display device according to claim 1, wherein the neck region ~~first extended portion at the boundary with the active layer~~ has a width narrower than the active layer.

7. (Currently Amended): The liquid crystal display device according to claim 6, wherein the width of the neck region ~~first extended portion at the boundary with the active layer~~ is in a range of about 2.8 μm (micrometers) to about 3.4 μm (micrometers).

8. (Currently Amended): The liquid crystal display device according to claim 7, wherein the drain electrode completely covering the neck region ~~first extended portion at the boundary~~

~~with the active layer~~ has a width in a range of about 4.5 μm (micrometers) to about 5.6 μm (micrometers).

9. (Original): The liquid crystal display device according to claim 1, further comprising a doped semiconductor layer between the semiconductor layer and the source electrode, and between the semiconductor layer and the drain electrode in the thin film transistor.

10. (Original): The liquid crystal display device according to claim 9, wherein the doped semiconductor layer is formed of doped amorphous silicon.

11. (Withdrawn): A method of fabricating a liquid crystal display device having an array substrate, comprising:

forming a gate line on a substrate;

forming a data line crossing the gate line and defining a pixel area;

forming a thin film transistor connected to the gate line and the data line, the thin film transistor having a gate electrode connected to the gate line, a source electrode over the gate electrode and connected to the data line, a drain electrode spaced apart from the source electrode, and a semiconductor layer having an active layer over the gate electrode and a first extended portion completely covered with the drain electrode at a boundary between the active layer and the first extended portion, wherein the first extended portion is disposed over the gate electrode; and

forming a pixel electrode in the pixel area, the pixel electrode electrically connected to the drain electrode.

12. (Withdrawn): The method according to claim 11, wherein the source electrode has a U-shape and surrounds a part of the drain electrode.

13. (Withdrawn): The method according to claim 12, wherein the part of the drain electrode has a rod shape.

14. (Withdrawn): The method according to claim 11, further comprising a second extended portion corresponding to the data line in the semiconductor layer.

15. (Withdrawn): The method according to claim 11, wherein the semiconductor layer is formed of amorphous silicon.

16. (Withdrawn): The method according to claim 11, wherein the first extended portion at the boundary with the active layer has a width narrower than the active layer.

17. (Withdrawn): The method according to claim 16, wherein the width of the first extended portion at the boundary with the active layer is in a range of about 2.8 μm (micrometers) to 3.4 μm (micrometers).

18. (Withdrawn): The method according to claim 17, wherein the drain electrode completely covering the first extended portion at the boundary with the active layer has a width in a range of about 4.5 μm (micrometers) to 5.6 μm (micrometers).

19. (Withdrawn): The method according to claim 11, further comprising a doped semiconductor layer between the semiconductor layer and the source electrode, and between the semiconductor layer and the drain electrode in the thin film transistor.

20. (Withdrawn): The method according to claim 19, wherein the doped semiconductor layer is formed of doped amorphous silicon.

21. (Withdrawn): A method of fabricating for a liquid crystal display device having an array substrate, comprising:

forming a gate line and a gate electrode on a substrate;

forming a gate insulating layer on the gate line and the gate electrode;

forming a semiconductor layer on the gate insulating layer, the semiconductor layer having an active layer over the gate electrode and a first extended portion, wherein the first extended portion at a boundary with the active layer is disposed over the gate electrode;

forming a data line, a source electrode, and a drain electrode on the semiconductor layer, the data line crossing the gate line and defining a pixel area, the source electrode disposed over

the gate electrode and connected to the data line, the drain electrode spaced apart from the source electrode and completely covering the first extended portion of the semiconductor layer at a boundary between the first extended portion and the active layer;

forming a passivation layer on the data line, the source electrode, and the drain electrode; and

forming a pixel electrode in the pixel area on the passivation layer, the pixel electrode connected to the drain electrode.